AGRESSOR AWARE DESIGN FOR BETTER IR-DROP RESULTS

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MOTIVATION

- AN IR-DROP AGGRESSOR IS A CELL THAT INDUCES IR-DROP ON NEIGHBORS WHEN IT IS DRAWING CURRENT FROM THE POWER-GRID.
- THE AGGRESSION IMPACT IS CORRELATED TO OVERLAPPING TIMING-WINDOWS.
- IN ADVANCED TECHNODES, THE IMPACT OF AGGRESSOR RELATED IR-DROP IS BECOMING A DOMINANT EFFECT, AND IS LINKED TO A RESISTIVE COUPLING BETWEEN CELLS THROUGH THE POWER-GRID, THIS EFFECT CAN BE CALLED CROSS-IMPEDANCE.

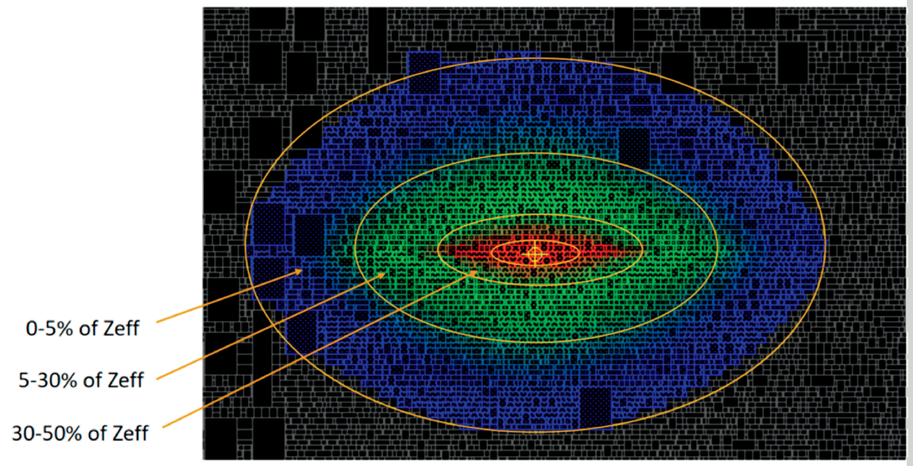


Image A: Electrical Impact zone on a single victim from neighboring aggressors. Data from Ansys study on advanced technology designs.

RESULTS

EARLY DESIGN STAGES

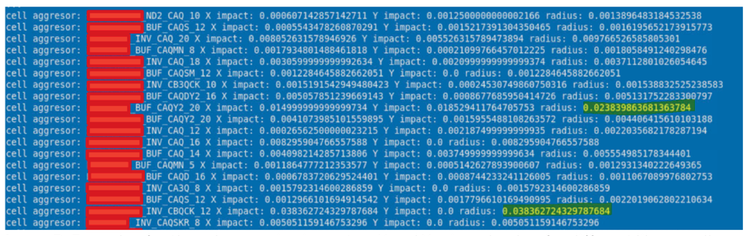


Image B: Example of gathered aggression impact on X and Y axis and radius for different library cells.

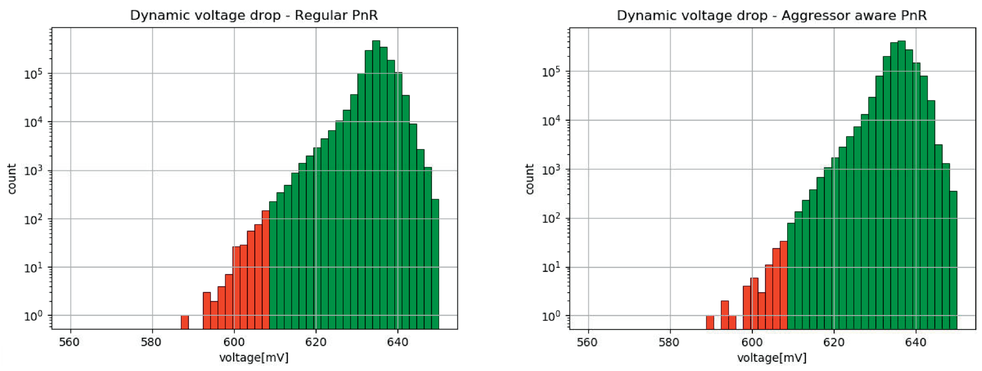


Image C: Dynamic IR-drop results Histograms on design before and after Aggressor aware rules. There is a reduction of ~350 IRdrop violations with the new rules.

	Regular PnR Flow		Aggressor Aware PnR	
	Setup	Hold	Setup	Hold
WNS	-0.025	-0.189	-0.044	-0.115
TNS	-2.286	-27.908	-4.782	-22.603
NVE	567	1695	981	1368

Image D: Timing Summary @ chip-finish stage for both runs (pre-optimization)

LATE DESIGN STAGES

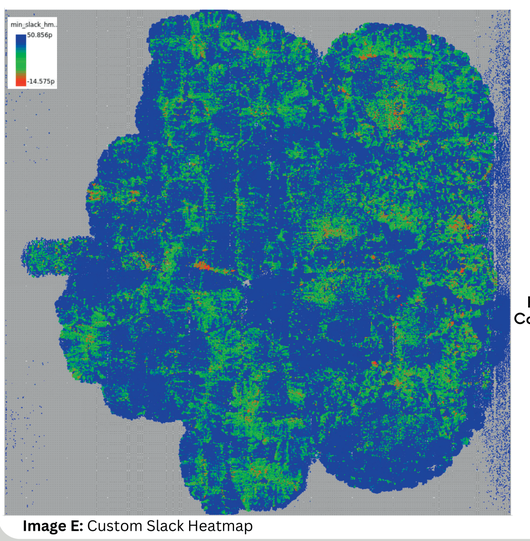


Image E: Custom Slack Heatmap

Heatmap Combination

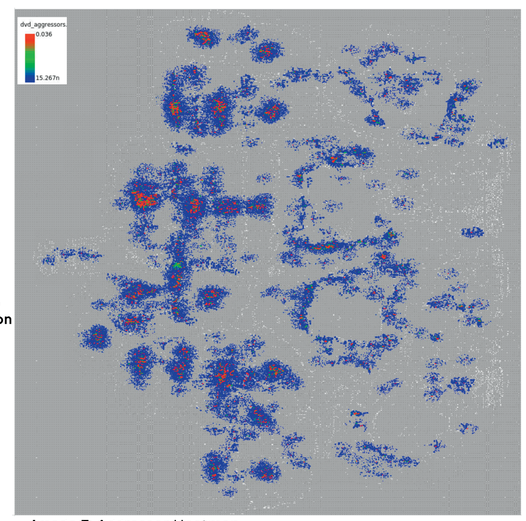


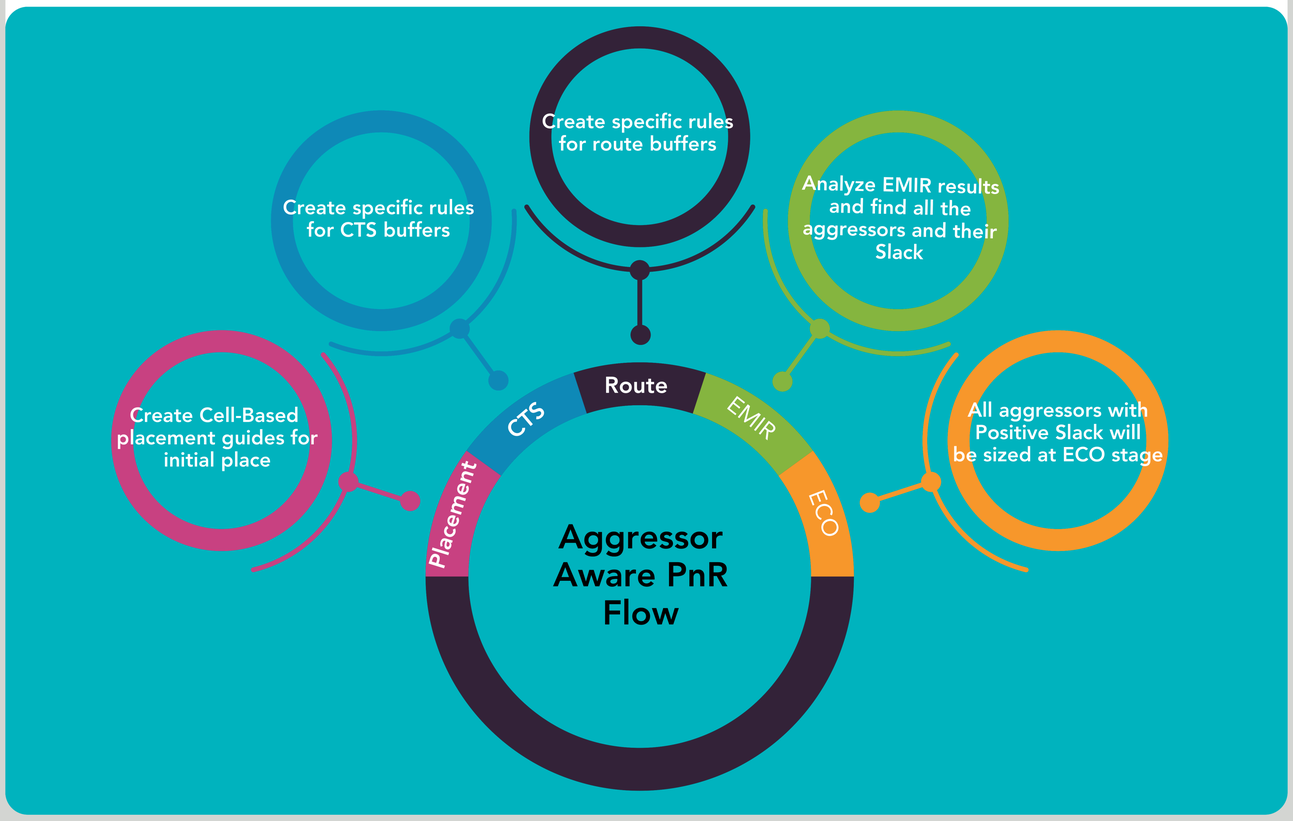
Image F: Aggressor Heatmap

METHODOLOGY

CREATING AN AGGRESSOR AWARE PNR FLOW THAT WILL OPTIMIZE THE DESIGN WHILE REDUCING THE IR-DROP.

- EARLY DESIGN STAGES: BY LEVERAGING THE ANSYS REDHAWK-SC PLATFORM, IT IS POSSIBLE TO CALCULATE THE IR-AGGRESSIVE IMPACT OF EVERY CELL IN THE LIBRARY FOR X AND Y DIRECTIONS. THIS CAN BE TRANSFORMED INTO ASYMMETRIC SET OF PLACEMENT BLOCKAGES THAT ALLOW TO MAXIMIZE THE CELL PLACEMENT WHILE MAINTAINING LOW IR-DROP.

- LATE DESIGN STAGES: WE CAN IDENTIFY ALL THE AGGRESSORS IN A MATURE DESIGN, AND BY USING THE SEASCAPE PLATFORM CAPABILITIES WE CAN COMBINE SLACK DATA ALONG WITH AGGRESSION IMPACT AND CREATE A SMALL SET OF POTENTIALLY "FREE" ECO'S WHERE AGGRESSORS WITH POSITIVE SLACK ARE IMMEDIATELY IDENTIFIED AND PASSED TO THE ECO FLOW FOR CELL SIZING.



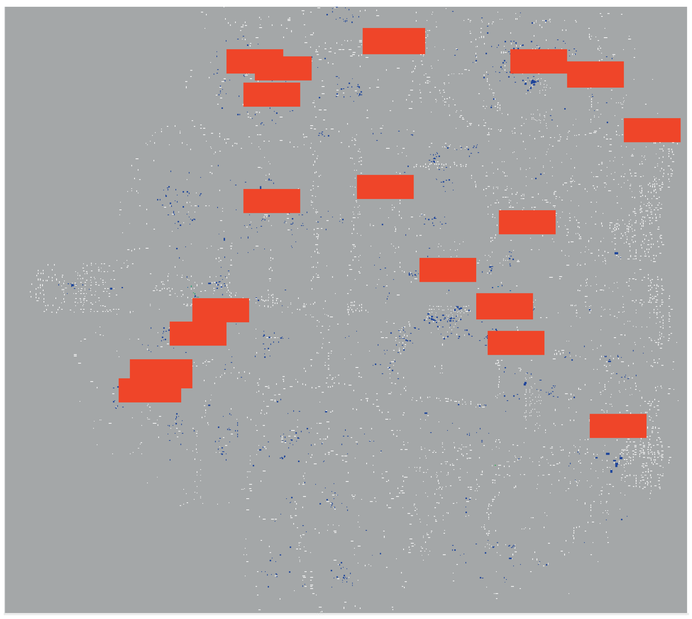


Image G: Filtered Potential Aggressors

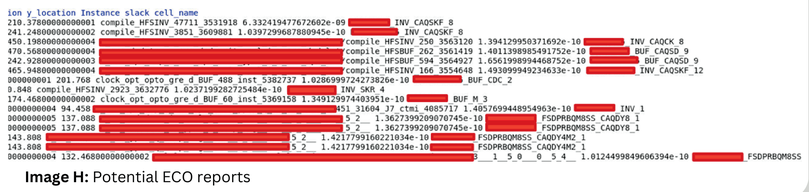


Image H: Potential ECO reports

FUTURE-STAGES

1. CREATE A LOGICALLY AWARE ECO ESTIMATOR TO MAKE SURE THAT NO 2 CELLS ARE BEING SIZED ON THE SAME LOGICAL PATHS THAT WILL CAUSE PATH TO FAIL TIMING.
2. CREATE AN ECO DELAY ESTIMATOR THAT WILL CALCULATE THE CELL-DELAY CHANGES IN THE CELL SIZING PROPOSAL AND WILL CHECK THE TIMING DEGRADATION TO EVALUATE THE ECO FEASIBILITY.
3. CREATE MULTI-CORNER FLOW THAT WILL TAKE INTO ACCOUNT ALL THE NEEDED CORNERS TO MAKE SURE THAT THE ECO PROPOSALS WILL BE VALID FOR ALL NEEDED CORNERS.